

**Notice of References Cited**

Application/Control No.

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Patent(s)/Patent Under

Re: Examination  
WALKER ET AL.

Examiner

Toniae M Thomas

Art Unit

2822

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-4,843,025 B1	06-1989	Morita	438/388
	B	US-4,918,499 B1	04-1990	Matsutani et al.	257/304
	C	US-5,343,354 B1	08-1994	Lee et al.	361/322
	D	US-5,346,845 B1	09-1994	Jun	438/244
	E	US-6,114,216 B1	09-2000	Yieh et al.	438/424
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 63-001052 A	01-1988	JP	Kimura et al.	H01L 027/10
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	<del>Wolf et al., "Chemical Vapor Deposition of Amorphous and Polycrystalline Films", Silicon Processing for the VLSI Era - Vol. 1: Process Technology, Lattice Press, 1986, pages 181-182.</del>
	V	Wolf et al., "Semiconductor Memory Process Integration", Silicon Processing for the VLSI Era - Vol. 2: Process Integration, Lattice Press, 1990, page 602.
	W	Wolf et al., "Isolation Technologies for Integrated Circuits", Silicon Processing for the VLSI Era - Vol. 2: Process Integration, Lattice Press, 1990, page 48.
	X	Wolf et al., "Hot Carrier-Resistant Processing and Device Structures", Silicon Processing for the VLSI Era - Vol. 3: The Submicron MOSFET, Lattice Press, 1995, pages 634-636.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.